

FIG.1

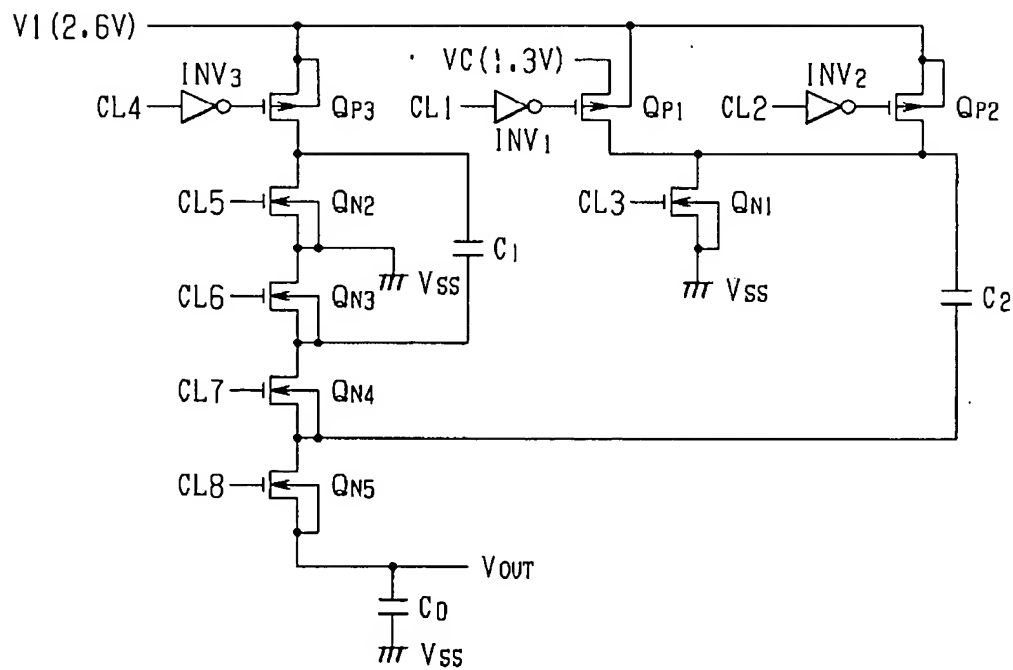


FIG.2

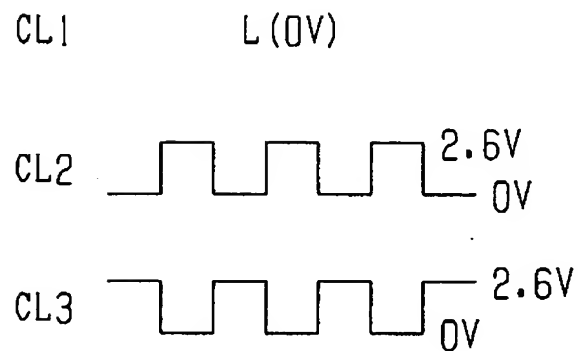


FIG.5

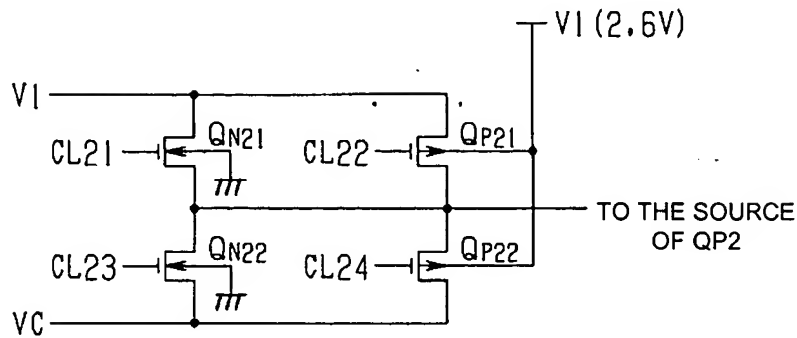


FIG.6

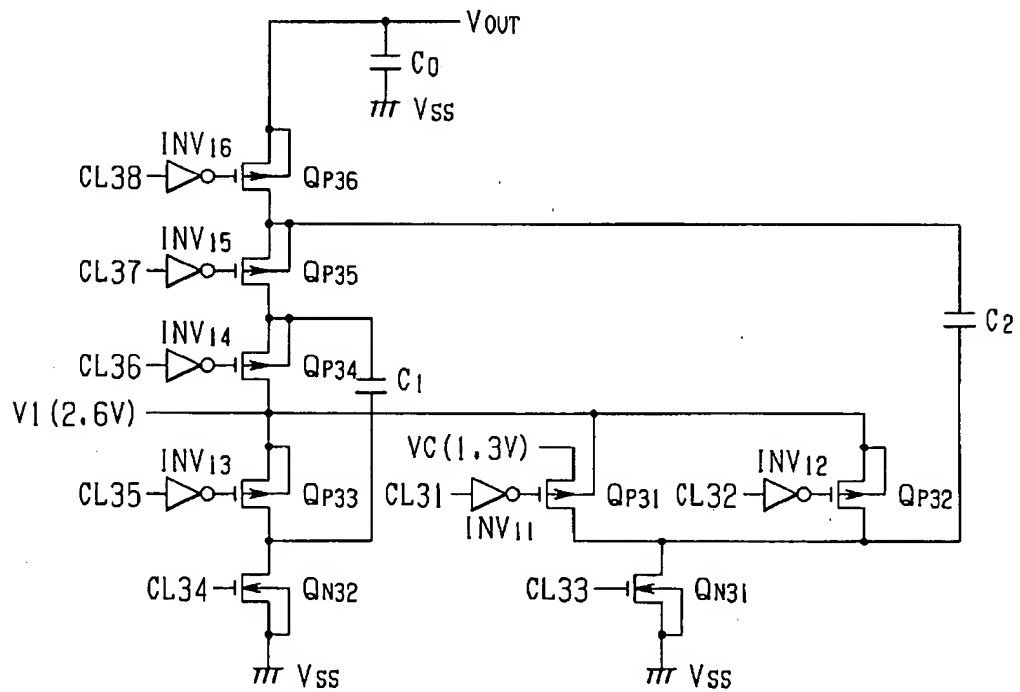


FIG.7

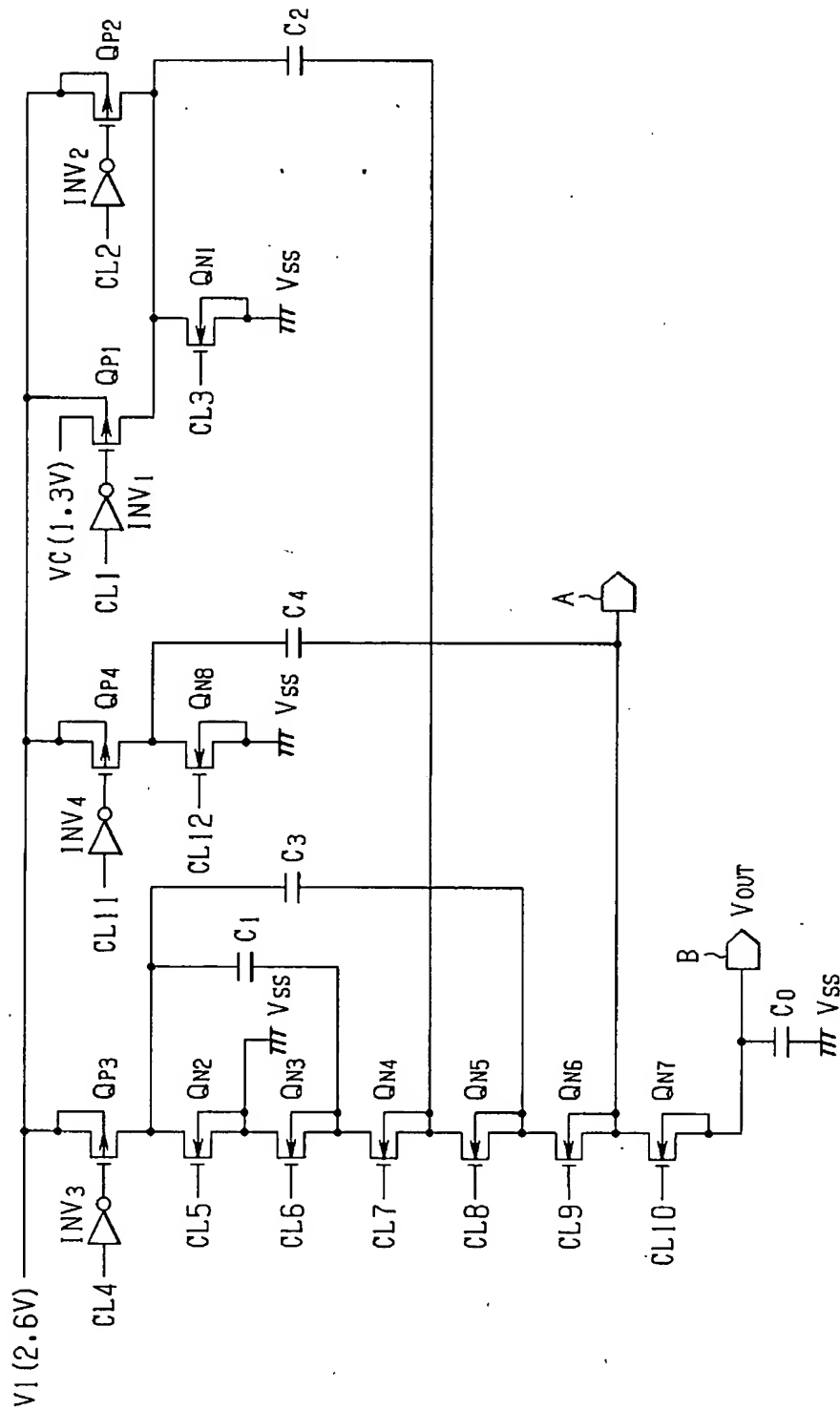


FIG.8

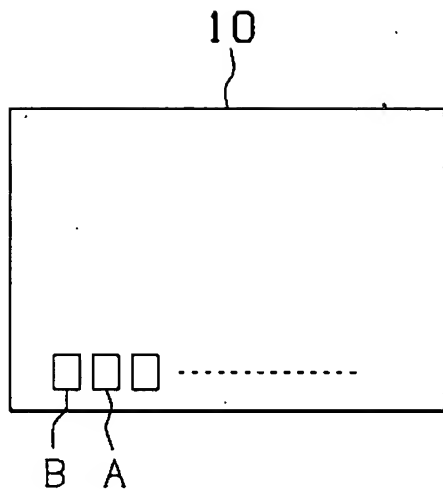


FIG.9

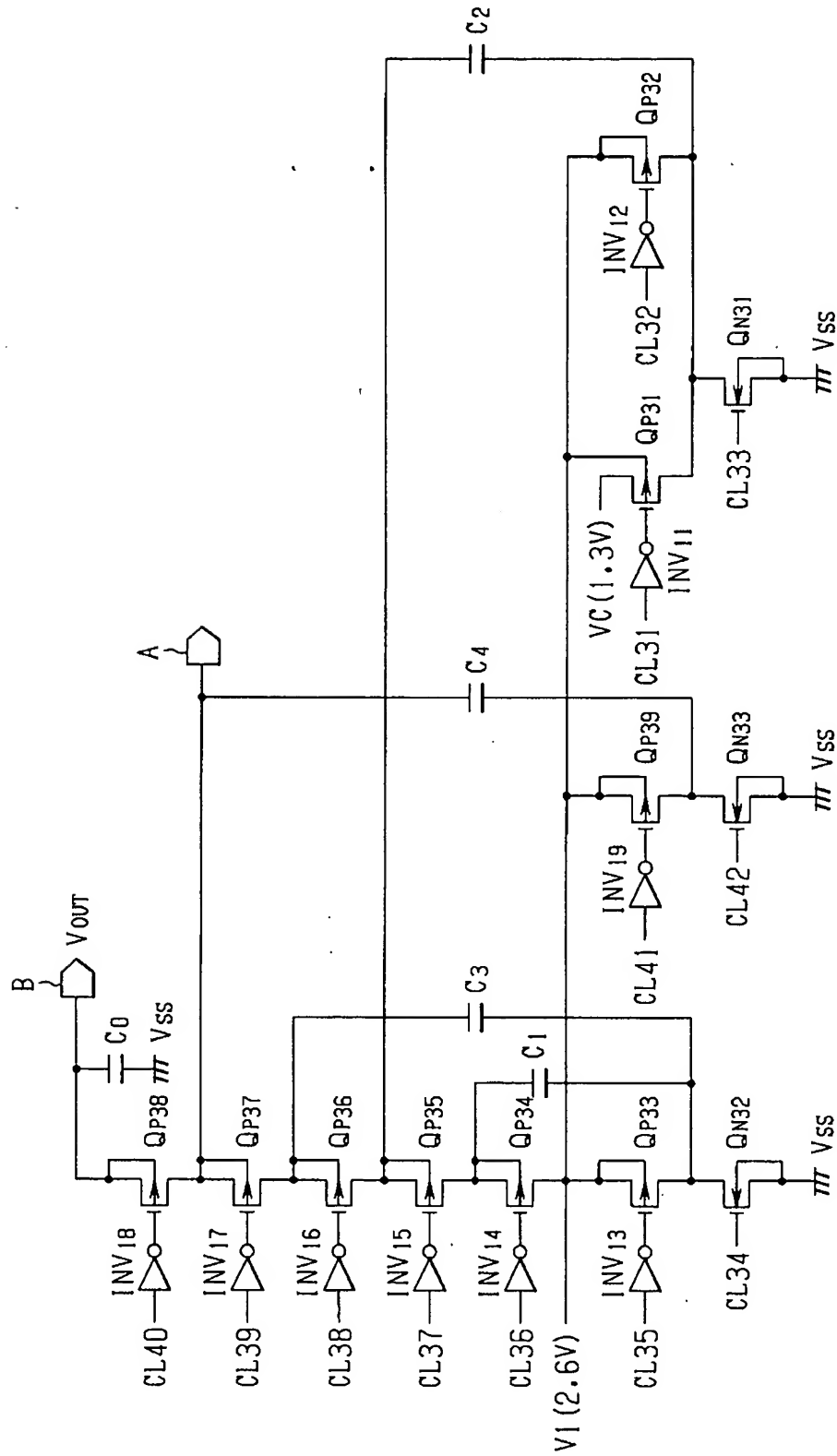


FIG.10 (A)

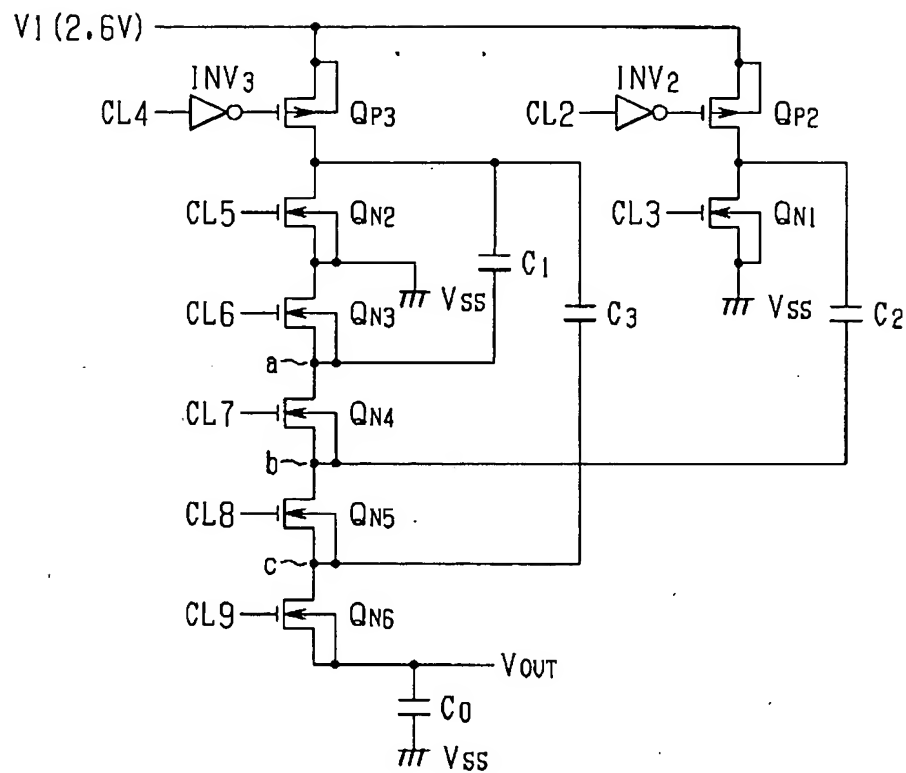


FIG.10 (B)



FIG.11

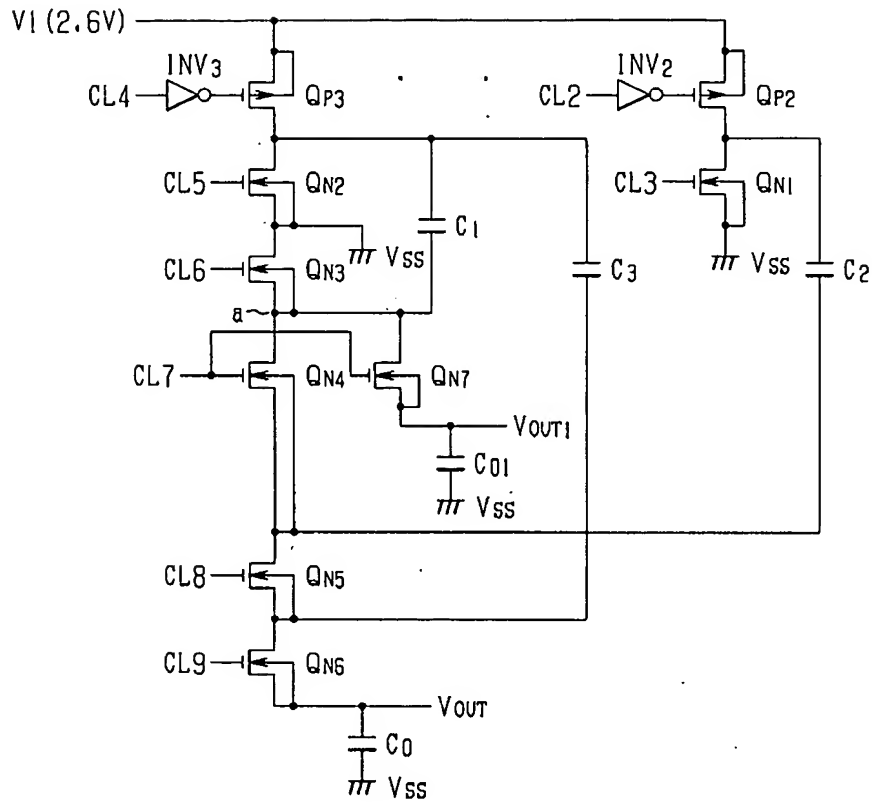


FIG.12

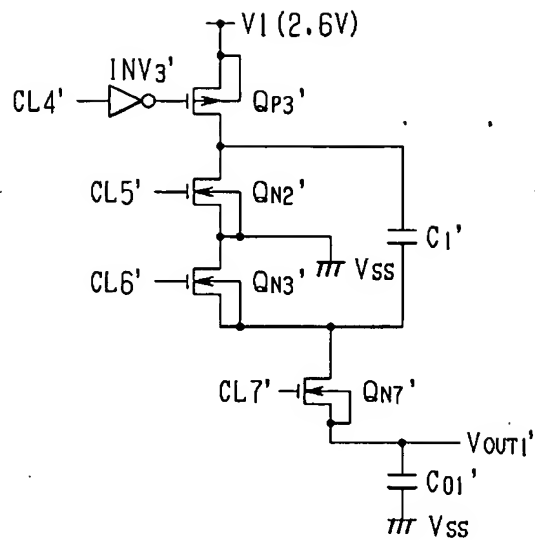
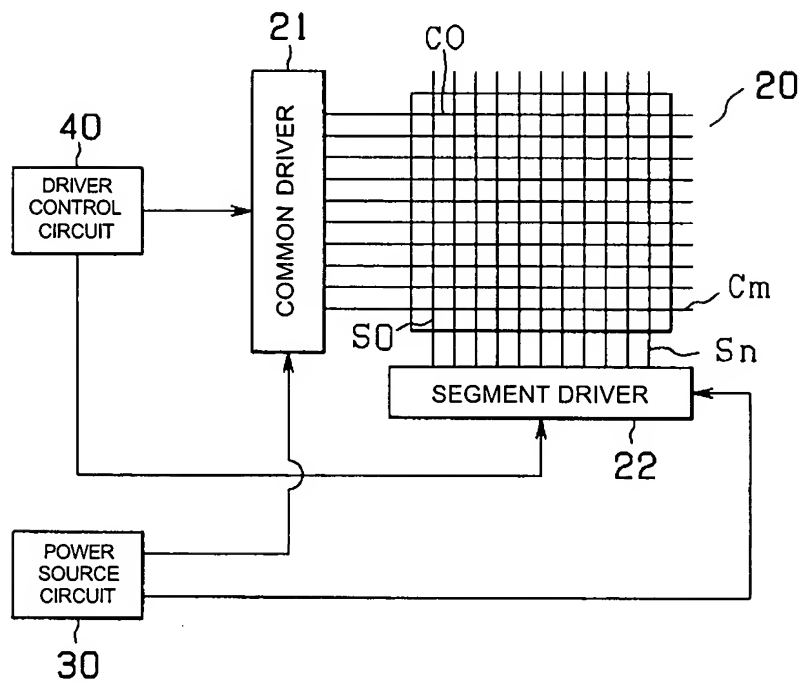


FIG.13



The diagram shows a 4-input CMOS NAND gate. The output node is connected to $V_1 (=2V_c)$ through capacitor C_0 and to V_{SS} through capacitor C_1 . The input nodes are connected to V_C through inverters INV_{21} , INV_{22} , INV_{23} , and CL_{51} . The output node is also connected to V_{SS} through a network of transistors QP_{51} , QP_{52} , QP_{53} , and QN_{51} .

FIG. 15

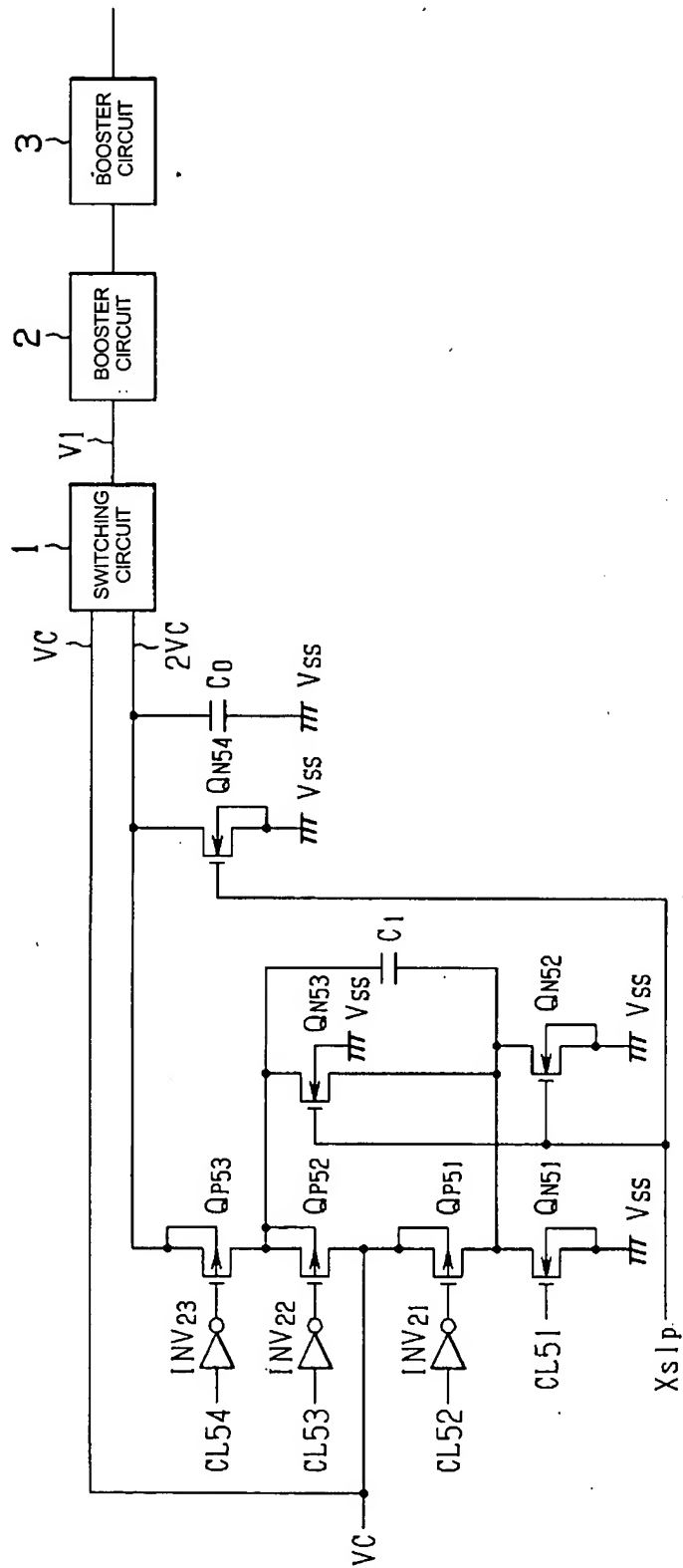


FIG.16

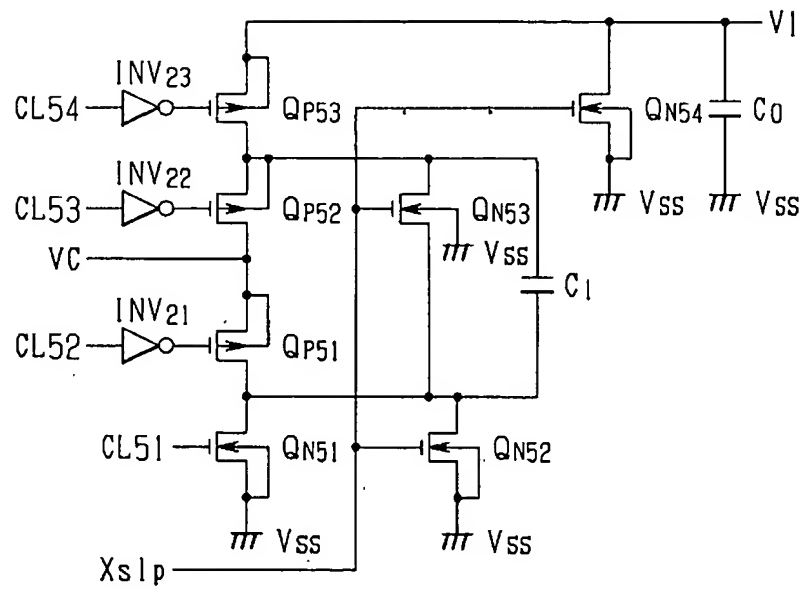


FIG.17

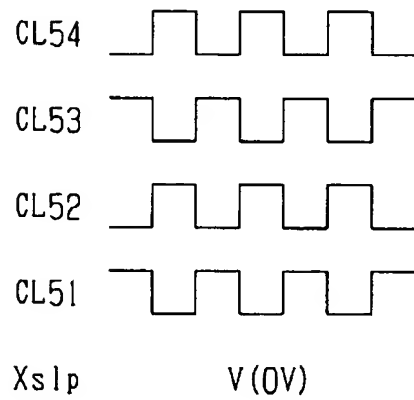


FIG.18

